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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,009	11/05/2001	Fereidoon Heydari	01-S-023 (1678-39)	8816

30431 7590 02/02/2009

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2627	

MAIL DATE	DELIVERY MODE
02/02/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/994,009	HEYDARI ET AL.	
	Examiner	Art Unit	
	Daniell L. Negrón	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-30 and 32-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-30 and 32-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed July 21, 2008 have been fully considered but they are not persuasive. Regarding claims 1-8, 10-23, 27, 28, 30, 32, and 33, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the claims indicate one of two representational schemes if four bits are to be used to represent a single bit (a "1/4" code): either a '1' and '0' are respectively represented by the consecutive bit sequences '0011' and '0000', or by the consecutive bit sequences '1100' and '1111') are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).
Regarding claims 24-26, 29, and 34, on page 20, Applicant argues that Examiner's obviousness rejection fails because the reference, Kuki "was, in fact motivated to improve the signal-to-noise ratio involved (column 3, lines 12-17) and yet did not teach or suggest the consecutive bit sequences according to the recitations of claim 24. Applicant further argues that Kuki intended Table II to be a comprehensive listing of acceptable four-bit encoding schemes and yet excluded the bit sequences of claim 24. However, Applicant is reminded that the rejection of claim 24 is of obviousness in view of the cited reference. Examiner's rationale is modifying the prior art in view of disclosure which is reasoned from knowledge generally available to one of ordinary skill in the art. The limitations which Applicant argues is not disclosed in Kuki, have already been identified by the Examiner as not explicitly disclosed by said reference. Applicant has not argued as to why it would not have been obvious to one having ordinary skill in the art at the

time of Applicant's invention to rearrange the logical states in Kuki et al to achieve the predictable result of improving the signal-to-noise ratio of the servo data by rearranging the logical states disclosed by Kuki.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-7, 10-23, 27-28, 30, and 32-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Kuki et al (US 6,233,715 B1).

Regarding claim 1, Kuki et al disclose a digital storage system, storing data, the data including a coded binary sequence, comprising a first group of consecutive bits, the first group having first and second separate (i.e. nonoverlapping) portions and representing one of logic 1 and a logic 0, the bits in the first portion each having a first state and the bits in the second portion each having a second state (col. 6, Table II, Case 6, NRZI Encoded Data "1"); and a second group of consecutive bits separate from the first group and each having the first state, the second group representing only the other of the logic 1 and the logic 0 (col. 6, Table II, Case 6, NRZI Encoded Data "0").

Regarding claims 2 and 7, Kuki et al disclose that the first and second portions of the first group (which is the second group in claim 7) respectively comprise first and second halves of the first group (col. 6, Table II, Case 6, NRZI Encoded Data "1").

Regarding claim 3, Kuki et al disclose that the first and second groups respectively represent logic 1 and logic 0 (col. 6, Table II, Case 6, NRZI Encoded Data “1”, “11” and “00” respectively represent logic 1 and logic 0).

Regarding claim 4, the limitations at this claim are met based on the sections of Kuki et al cited above in the rejection of claim 1.

Regarding claim 5, Kuki et al disclose that the first and second groups respectively represent logic 0 and logic 1 (see the rejection of claim 1 above); and the first and second states respectively equal logic 0 and logic 1 (col. 6, Table II, Case 6, NRZI Encoded Data "1").

Regarding claim 6, Kuki et al disclose that the first and second groups each respectively comprise four consecutive bits (col. 6, Table II, Case 6).

Regarding claims 10, 16, and 19, Kuki et al disclose a disk drive system comprising: a storage disk (Fig. 1, 12) having disk sectors operable to store application data (Fig. 2, data sectors); and servo wedges that store servo data (Fig. 2, servo sectors) that includes the format claimed in claim 10 (which is equivalent to the coded binary sequence of claim 1) (Fig. 2, 66; Table II, Gray Code). It is inherent in Kuki et al that there be a motor coupled to and operable to rotate the disk given that the disk is rotating as shown in Figure 1. Kuki et al further disclose a read/write head operable to generate a servo signal that represents the servo data and having a position with respect to the surface of the storage disk (Fig. 1, 14); a read-head positioning circuit operable to move the read head over the surface of the disk (Fig. 1, 34); and a servo circuit coupled to the read head and operable to recover the servo data from the servo signal (Fig. 1, 30, 32).

Regarding claims 11-13, Kuki et al disclose a Viterbi detector (Fig. 1, 28) comprising an input node operable to: receive a signal that represents a coded binary sequence as claimed in claims 11-13 (which is equivalent to the coded binary sequence of claims 1 and 4); and a circuit coupled to the input node and operable to recover the binary sequence from the signal (Fig. 7, 1/4 Code, EPR4EQ, EPR4Viterbi w/ECU).

Regarding claims 14 and 17, Kuki et al disclose a servo circuit, comprising: a sample circuit operable to generate samples of a signal that represents a coded binary sequence as claimed in claim 14 (which is equivalent to the coded binary sequence of claims 1 and 4) (Fig. 1, 22); and a Viterbi detector coupled to the sample circuit and operable to recover the coded binary sequence from the samples of the signal (see the rejection of claims 11-13 above).

Regarding claims 15 and 18, it is inherent in Kuki et al that there be a decoder coupled to the Viterbi detector operable to decode the recovered binary sequence since data that is encoded as Gray code data of necessity must be decoded once a Viterbi detector has detected the Gray code data.

Regarding claims 20 and 23, Kuki et al disclose a method, comprising: coding one of a logic 1 and a logic 0 as a first group of consecutive bits, the first group having first and second equally sized portions that respectively comprise first and second halves of the first group, the bits in the first portion each having a first state and the bits in the second portion each having a second state (col. 6, Table II, Case 6, NRZI Encoded Data "1"); and coding the other and only the other of the logic 1 and the logic 0 as a second group of consecutive bits separate from the first group and each having the first state (col. 6, Table II, Case 6, NRZI Encoded Data "0").

Regarding claim 21, Kuki et al disclose that the first and second groups respectively represent a logic 1 and a logic 0 (col. 6, Table II, Case 6, NRZI Encoded Data "1"; "11" and "00" respectively represent a logic 1 and a logic 0); the first and second states respectively equal logic 0 and logic 1 (col. 6, Table II, Case 6, NRZI Encoded Data "1").

Regarding claim 22, Kuki et al disclose coding the one of the logic 1 and the logic 0 as a first group of four consecutive bits; and coding the other of the logic 1 and the logic 0 as a second group of four consecutive bits (col. 6, Table II, Case 6).

Regarding claim 27, Kuki et al disclose a method, comprising: writing a first code symbol into a servo wedge of a data-storage disk (Fig. 2, Servo, 66), the first code symbol having a first group of code bits and a second group of code bits, having a length and representing one of a logic 1 and a logic 0, each bit in the first group having a first value and each bit in the second group having a second value that is different than the first value (col. 6, Table II, Case 6, NRZI Encoded Data "1"); and writing a second code symbol into the servo wedge, the second code symbol having the length or approximately the length, having a single group of code bits each having the first value, and representing only the other of the logic 1 and the logic 0 (col. 6, Table II, Case 6, NRZI Encoded Data "0").

Regarding claim 28, Kuki et al disclose that the first and second code symbols each comprise a first number of bits (col. 6, Table II, Case 6, 4 code bits); the servo wedge comprises a second number of bits and the lengths of the first and second code symbols (i.e. 4 code bits) are each less than the product of the first and second numbers (col. 6, Table II, Case 6).

Regarding claim 30, Kuki et al disclose that each of the first and second groups of code bits is or is approximately half as long as the first code symbol (col. 6, Table II, Case 6, 2 bits vs. 4 bits).

Regarding claims 32-33, Kuki et al disclose a coded binary sequence, comprising: a first group of consecutive bits, the first group having first and second portions and representing one of a logic 1 and a logic 0, the first portion preceding the second portion, the bits in the first portion each having a first state and the bits in the second portion each having a second state (col. 6, Table II, Case 6, NRZI Encoded Data "1"); and a second group of consecutive bits each having the first state, the same state being the first state or the second state, the second group representing only the other of the logic 1 and the logic 0 (col. 6, Table II, Case 6, NRZI Encoded Data "0").

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 24-26, 29, 34, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuki et al (US 6,233,715 B1).

Regarding claim 24, Kuki et al disclose a method, comprising: coding a first logical bit of servo data and only the first logical bit as a first group of four consecutive bits each having a first logic level, the first logical bit representing the first logic level or a second logic level (col. 6, Table II, Case 6, NRZI Encoded Data "0"; the first logical bit represents the first logic level).

Kuki et al further disclose coding a second logical bit of servo data as a second group of four consecutive bits, the second logical bit representing the first logic level if the first logical bit represents the second logic level, the second logical bit representing the second logic level if the first logical bit represents the first logic level (col. 6, Table II, Case 6, NRZI Encoded Data "1"; the first logical bit represents the first logic level and the second logical bit represents the second logic level).

However, Kuki et al do not disclose that the second group of four consecutive bits respectively have the first logic level, the first logic level, the second logic level, and the second logic level ("0011"); rather, Kuki et al disclose that the second group of four consecutive bits respectively have the second logic level, the second logic level, the first logic level, and the first logic level ("1100"). Having said that, a rearrangement of logical states without any unexpected results is not patentably distinguishing subject matter (there would be no unexpected results in this case since the logic 1 bits simply take the space of the logic 0 bits and vice versa). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to rearrange the logical states in Kuki et al to achieve the predictable result of improving the signal-to-noise ratio of the servo data (Kuki et al, col. 7, lines 21-28; specification, paragraph 2).

Regarding claim 25, Kuki et al disclose that the first logical bit equals a logic 0; and the second logical bit equals a logic 1 (see the above rejection of claim 24).

Regarding claim 26, the limitations at this claim are met based on the discussion of claim 24 above.

Regarding claim 29, Kuki et al disclose the limitations at claim 27 as discussed above. Kuki et al fail to disclose that the first code symbol represents a logic 0; and the second code

symbol represents a logic 1; rather, Kuki et al disclose that the first code symbol represents a logic 1; and the second code symbol represents a logic 0. Having said that, a rearrangement of logical states without any unexpected results is not patentably distinguishing subject matter. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to rearrange the logical states in Kuki et al to achieve the predictable result of improving the signal-to-noise ratio of the servo data (Kuki et al, col. 7, lines 21-28; specification, paragraph 2).

Regarding claim 34, Kuki et al disclose the limitations at claim 33 as discussed above. Kuki et al further disclose that the first group represents a logic 1 (col. 6, Table II, Case 6, NRZI Encoded Data "1"); each bit of the second group has the first state (Table II, Case 6, "0000"); and the second group represents a logic 0 (Table II, Case 6, NRZI Encoded Data 0).

However, Kuki et al fail to disclose that the first state comprises a logic 0; and the second state comprises a logic 1; rather, they teach the opposite. Having said that, a rearrangement of logical states without any unexpected results is not patentably distinguishing subject matter. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to rearrange the logical states in Kuki et al to achieve the predictable result of improving the signal-to-noise ratio of the servo data (Kuki et al, col. 7, lines 21-28; specification, paragraph 2).

Regarding claim 35, claim 35 has limitations similar to those treated in the above rejections of claims 33 and 34, and are met by the reference as discussed above.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniell L. Negrón whose telephone number is (571)272-7559. The examiner can normally be reached on Monday-Friday (8:30am-5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joseph H. Feild can be reached on (571) 272-4090. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Joseph H. Feild/
Supervisory Patent Examiner, Art Unit 2627

/Daniell L. Negrón/
Examiner, Art Unit 2627
January 26, 2009